In the claims:

Please substitute the following full listing of claims, including new claim 45, for the claims as originally filed or most recently amended.

1. (Currently Amended) A ~~An emitter controlled~~ thyristor device package having a cathode terminal and an anode terminal, comprising:

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

a first discrete metal oxide semiconductor (MOS) transistor connected in series with said thyristor between said cathode terminal and said thyristor emitter;

a second discrete MOS transistor connected between said cathode terminal and said thyristor gate~~, a gate terminal of said second MOS transistor connected to said cathode terminal~~; and

means for injecting ~~electrons~~ current into said thyristor gate for triggering said thyristor into a latching state;

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode terminal turning said ~~emitter controlled~~ thyristor device package to an on state, and a zero to second voltage applied to said gate of said first MOS transistor turns said ~~emitter controlled~~ thyristor device package to an off state.

2. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 1 further comprising a floating ohmic contact (FOC) for shorting said emitter and a source terminal of said first MOS transistor.

3. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 1 further comprising a metal strap for shorting said thyristor emitter and a source terminal of said first MOS transistor.

4. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 1, further comprising:

a third MOS transistor having a source and a drain connected between said thyristor emitter and a thyristor lower base region, and

a gate connected to said cathode terminal.

5. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 1 wherein said first MOS transistor comprises a PMOS transistor, and said second MOS transistor comprises a PMOS transistor.

6. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 4 wherein said first MOS transistor comprises a PMOS transistor, said second MOS transistor comprises a PMOS transistor, and said third MOS transistor comprises an NMOS transistor.

7. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 4 wherein said first MOS transistor comprises a NMOS transistor, said second MOS transistor comprises a PMOS transistor, and said third MOS transistor comprises an NMOS transistor.

8. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 4, further comprising

a metal strap for shorting said thyristor emitter with one of a drain and source terminal of said first MOS transistor.

9. (Currently Amended) A ~~An emitter controlled~~ thyristor device package as recited in claim 1, further comprising

a diode connected between said gate of said first MOS transistor and said thyristor emitter.

10. - 18. (Previously Canceled)

19. (Currently Amended) A ~~gate turn-off (GTO)~~ thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal plate;

a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said ~~GTO~~ thyristor device package;

a first discrete metal oxide semiconductor (MOS) transistor positioned on said second metal plate adjacent said thyristor, said first MOS transistor having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for said ~~GTO~~ thyristor device package; and

a second discrete MOS transistor positioned on said second metal plate adjacent said thyristor, said second MOS transistor having a first terminal connected to a gate of said thyristor, said second MOS transistor further having a second terminal ~~and a gate terminal~~

connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns said thyristor device to an off state.

20. (Currently Amended) A ~~gate turn-off (GTO)~~ thyristor device package as recited in claim 19, further comprising a clamp means for holding said first, second and third metal plates together.

21. (Currently Amended) A ~~gate turn-off (GTO)~~ thyristor device package as recited in claim 19, wherein said first, second and third metal plates comprise copper plates.

22. (Currently Amended) A ~~gate turn-off (GTO)~~ thyristor device package as recited in claim 19, wherein ~~said first and second discrete semiconductor switches are first and second MOS transistors, respectively, and~~ said first MOS transistor and said second MOS transistor are complementary.

23. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package comprising:

a gate turn-off (GTO) thyristor comprising a thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a first plurality of discrete switching devices connected in parallel and arranged in a circular fashion around said GTO thyristor, a first terminal of said first plurality of discrete switching devices connected to said thyristor emitter and a second terminal of said first plurality of discrete switching devices connected to a cathode terminal of said ~~GTO~~

thyristor device package; and

a second plurality of discrete switching devices connected in parallel and arranged in a circular fashion around said GTO thyristor, a first terminal of said second plurality of discrete switching devices connected to said thyristor gate and a second terminal of said second plurality of discrete switching devices connected to said cathode terminal of said GTO device package,

wherein a first voltage applied to ~~a~~ gate ~~terminal~~ terminals of said first plurality of discrete switching devices turns said GTO thyristor to an on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate terminals of said first plurality of discrete switching devices turns said GTO thyristor to an off state.

24. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23, further comprising:

a first metal plate forming said cathode terminal;

a second metal plate separated from said first metal plate by an insulation layer, wherein said GTO thyristor and ~~said MOS transistors and~~ said discrete switching devices of said first and second pluralities of discrete switching devices are positioned on said second metal plate, said first and second metal plates acting as a heat sink.

25. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 further comprising a third metal plate forming an anode terminal of said ~~GTO~~ thyristor device package.

26. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices ~~each~~ comprise ~~a~~ MOS ~~transistor~~ transistors having respective gates ~~a gate~~ connected to said cathode or gate terminal.

27. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a diode.

28. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a diode connected in parallel with a capacitor.

29. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a Zener diode connected in parallel with a capacitor.

30. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a transistor connected in parallel with a capacitor.

31. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 26 further comprising;

a first feedback path connecting said gate of said MOS transistors to said thyristor emitter; and

a second feedback path connecting said gate of said MOS transistors to said thyristor gate through a diode.

32. (Currently Amended) A ~~gate turn-off~~ thyristor ~~(GTO)~~ device package as recited in claim 23, further wherein said ~~first~~ discrete switching devices of said first plurality of discrete switching device comprise a MOS transistor, said thyristor device package further comprising:

a feedback path connecting said gate of said MOS transistor to said thyristor emitter;

a capacitor connected in parallel to said MOS ~~switching device~~ transistor connecting said second terminal of said MOS transistor to said thyristor gate.

33. - 37. (Previously Canceled)

38. (Currently Amended) A ~~An emitter turn-off~~ thyristor device package including

a thyristor element having an anode terminal, an emitter terminal and a gate terminal,

a first discrete semiconductor switch connected in series with said emitter terminal of said thyristor device by a first terminal of said first semiconductor switch,

a second discrete semiconductor switch connected in series with said gate terminal of said thyristor device by a first terminal of said second discrete semiconductor switch; second terminals of said first and second discrete semiconductor switches being connected together, and

means for shorting said emitter of said thyristor element to a terminal of said first discrete semiconductor switch or for injecting ~~electrons~~ current into said thyristor gate for triggering said thyristor into a latching state;

wherein said first and second discrete semiconductor switches are arranged such that a signal of a first type applied to said first discrete ~~electronic~~ semiconductor switch turns said ~~emitter turn-off~~ thyristor element to an on-state and a signal of a second type applied to said first ~~electronic~~ semiconductor switch turns said ~~emitter turn-off~~ thyristor element to an off-state, and

wherein at least one of said first and second semiconductor switches is constituted by a plurality of semiconductor devices.

39. - 44. (Previously Canceled)

45. (New) A thyristor device package as recited in claim 1, wherein

a gate terminal of said second MOS transistor is connected to said cathode terminal.

46. (New) A thyristor device package as recited in claim 19, wherein

said second discrete MOS transistor further includes a gate terminal connected to said third metal plate.